

09/317536

ABSTRACT OF THE INVENTION

A method is provided for forming an improved interconnect structure on a semiconductor body. A first metal layer is deposited on the semiconductor body. A sacrificial layer having a height is deposited on the first metal layer. The sacrificial layer and the metal layer are patterned to form separate metal lines with the sacrificial layer remaining on said metal lines. A low-k material is then deposited to fill the gaps between metal lines and to cover the sacrificial layer. The low-k material is then removed to a level within the height of the sacrificial layer. The sacrificial layer is then removed. A protective layer is deposited on top of the metal lines and the low-k material. A dielectric layer is deposited over the protective layer. The protective layer protects the low-k material from attack by chemicals utilized by subsequent process steps to etch vias in the dielectric layer, to strip photo-resist, and to clean the vias. The protective layer is then selectively etched away to make contact between a via plug and the metal lines.

09/317536